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EXAMINER
TANG, KENNETH

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Please find below and/or attached an Office communication concerning this application or proceeding.

5Y

Office Action Summary	Application No. 09/449,912	Applicant(s) DIVITTORIO, NICK P.
	Examiner Kenneth Tang	Art Unit 2127

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to Pre-Amendment A. This application is filed on 12/02/99. Claims 1-26 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 7 and 19 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The terminology "ratio block" is not explicitly defined in the specification.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 7 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The terminology "ration block" is indefinite.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 26 is rejected under 35 U.S.C. 102(e) as being unpatentable by Dailey (US 6,330,483 B1).

4. Referring to claim 26, Dailey teaches a multi-level multivariable industrial process control program execution framework for an industrial control processor including:

- a first cyclically executed sequence of instructions, repeatedly executed according to a first configurable repetition period and at a first level of execution priority, the first cyclically executed program executing a sequence of instructions including at least a set of instructions for calculating a setpoint value for a process control variable *["channel prioritization in multi-channel control systems", col. 5, lines 27-35, "priorities assigned via the Dailey L1 Optimization Algorithm cost function", col. 10, lines 7-17, "lowest priority", col. 13, lines 29-42, The present invention can address the relationships between primary and secondary controls. It is common for multi-variable control systems to designate certain control effectors as primary or secondary", col. 19, lines 46-64, see examples of linear algebraic multi-variable matrices with various setpoints in col. 15, lines 50-65, "linear control system", col. 11, lines 40-44, "linear gain matrices", col. 2, lines 46-57];*
- a second cyclically executed sequence of instructions, repeatedly executed according to a second repetition period and at a second level of execution priority, the second level of

priority exceeding the first level of priority, and thus enabling the control processor to temporarily suspend execution of the first cyclically executed sequence of instructions in order to execute the second cyclically executed sequence of instructions *["higher priority", "prioritization", "important for reasons of safety and system performance requirements", "optimal control system", "provides this protection by acting on the system's actual state, not just its operator's", col. 14, lines 24-38, "multi-channel aircraft control system", col. 2, lines 6-12, "primary controls", "secondary controls", "priorities", "allows the plant's full range of achievable control power to be exploited by a controller", col. 18, lines 22-42].*

It is inherent that the lower priority sequence would be suspended if the higher priority sequence is executed because that is the purpose of establishing priorities. It is also inherent that the sequences are cyclic *["begins a new iteration cycle", col. 38, lines 1-3].*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 5, 13-14, 17 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dailey (US 6,330,483 B1) as applied to claim 1 above, and further in view of Daggett et al. (hereinafter Daggett) (US 4,786,847).

5. Referring to claim 1, Dailey teaches a control processor for executing a set of control tasks defining dynamic model-based interactive control of an industrial process, the control processor comprising:

- an embedded control task, performed at a relatively low execution priority status within the control processor, the embedded control task comprising a multivariable linear program including a set of output values corresponding to process setpoints *["channel prioritization in multi-channel control systems", col. 5, lines 27-35, "priorities assigned via the Dailey L1 Optimization Algorithm cost function", col. 10, lines 7-17, "lowest priority", col. 13, lines 29-42, The present invention can address the relationships between primary and secondary controls. It is common for multi-variable control systems to designate certain control effectors as primary or secondary", col. 19, lines 46-64, see examples of linear algebraic multi-variable matrices with various setpoints in col. 15, lines 50-65, "linear control system", col. 11, lines 40-44, "linear gain matrices", col. 2, lines 46-57]*;
- a set of control blocks, performed at a relatively high execution priority status within the control processor, the set of control blocks including regulatory control blocks having output values that are transmitted by the control processors to field devices *["higher priority", "prioritization", "important for reasons of safety and system performance*

requirements", "optimal control system", "provides this protection by acting on the system's actual state, not just its operator's", col. 14, lines 24-38, "foreground task in the embedded control software", col. 37, lines 20-28, "multi-channel aircraft control system", col. 2, lines 6-12, "aircraft control system", col. 6, lines 1-7, "invention relates to control systems, and more particularly to real-time control systems for which an optimized output is desired", col. 1, lines 1-6, "primary controls", "secondary controls", "priorities", "allows the plant's full range of achievable control power to be exploited by a controller", col. 18, lines 22-42].

Dailey does teach both having control blocks having output values that are transmitted by the control processors to field devices coupled to the industrial process and also having a priority system *[see above]*. However, the reference of Dailey fails to explicitly teach the connection between having a high execution priority status and outputting the values from the control system to the industrial devices. However, Daggett teaches a control system that sets a high execution priority to the implementation of an industrial device *["SCM implementation, device U0096 has the highest priority", col. 39, lines 32-43]*. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have this connection/relationship between the two to the existing system of Dailey for the reason of maintaining functionality. It is well known that executing output values of a control system should be at a high priority because those values are needed for the system or industrial device to work.

6. Referring to claims 2 and 14, Daggett teaches the control processor of claim 1 wherein the set of control blocks comprise supervisory control blocks *["supervisory control", col. 8, lines 30-39, and "supervisory program execution", col. 70, lines 45-47].*

7. Referring to claims 5 and 17, Dailey teaches the method of claims 2 and 14, respectively, wherein the supervisory control blocks include at least one multivariable loop block, and further comprising the step of providing an input value for a regulatory control block in accordance with execution of instructions and data associated with the at least one multivariable loop block *[see examples of linear algebraic multi-variable matrices with various setpoints in col. 15, lines 50-65, "linear control system", col. 11, lines 40-44, "linear gain matrices", col. 2, lines 46-57, "multi-channel aircraft control system", col. 2, lines 6-12].*

8. Referring to claim 13, Dailey teaches a method for operating a control processor, in an industrial process control environment, to establish operating values including a set of setpoint values and a set of process control variables associated with control elements in a controlled industrial process based upon a set of input variables including process variables provided to the control processor and representing the present state of the controlled industrial process, the method comprising the steps of:

- executing at a lower execution priority, by the control processor, an embedded multivariable control application including computer instructions facilitating computing a setpoint value corresponding to a process control variable *["channel prioritization in multi-channel control systems", col. 5, lines 27-35, "priorities assigned via the Dailey L1*

Optimization Algorithm cost function", col. 10, lines 7-17, "lowest priority", col. 13, lines 29-4., The present invention can address the relationships between primary and secondary controls. It is common for multi-variable control systems to designate certain control effectors as primary or secondary", col. 19, lines 46-64, see examples of linear algebraic multi-variable matrices with various setpoints in col. 15, lines 50-65, "linear control system", col. 11, lines 40-44, "linear gain matrices", col. 2, lines 46-57];

- executing at a higher execution priority, by the control processor, a set of control blocks including regulatory control blocks for receiving and storing a set of process variables representing the present state of a controlled process *["higher priority", "prioritization", "important for reasons of safety and system performance requirements", "optimal control system", "provides this protection by acting on the system's actual state, not just its operator's", col. 14, lines 24-38, "multi-channel aircraft control system", col. 2, lines 6-12, "foreground task in the embedded control software", col. 37, lines 20-28, "aircraft control system", col. 6, lines 1-7, "invention relates to control systems, and more particularly to real-time control systems for which an optimized output is desired", col. 1, lines 1-6, "primary controls", "secondary controls", "priorities", "allows the plant's full range of achievable control power to be exploited by a controller", col. 18, lines 22-42].*

Dailey does teach both having control blocks having output values that are transmitted by the control processors to field devices coupled to the industrial process and also having a priority system *[see above]*. However, the reference of Dailey fails to explicitly teach the higher execution priority leading to the present state of a controlled process. However, Daggett teaches

a control system that sets a high execution priority, and when that occurs, an interrupt brings/resets the system to the current or present state *["SCM implementation, device U0096 has the highest priority", "common interrupt request signal", "interrupt", col. 39, lines 32-43].* It would have been obvious to one of ordinary skill in the art at the time the invention was made to have an interrupt when a high execution priority has occurred for the reason of maintaining functionality and improving accuracy of the system. It is well known that interrupts can interrupt the processing of a control system and redirect the current or present state to somewhere else.

9. Referring to claim 25, Dailey teaches an industrial process control computer having multiple operating level including:

- a background control program execution level wherein the process control computer executes an embedded multivariable process control application, the embedded control application including instructions for executing a multivariable linear program to generate a set of values corresponding to process control variable setpoints *["executed in the background at slower sample period", col. 37, lines 20-28, "channel prioritization in multi-channel control systems", col. 5, lines 27-35, see examples of linear algebraic multi-variable matrices with various setpoints in col. 15, lines 50-65, "linear control system", col. 11, lines 40-44, "linear gain matrices", col. 2, lines 46-57]*;

Dailey fails to explicitly teach:

- a foreground control block execution level wherein the process control computer executes a set of control blocks, at a higher execution priority level than the background control program execution level, the set of control blocks including program instructions

that, when executed, receive and store a set of process variable values representing the state of a controlled process

Dailey does teach a foreground control and that there are priorities of execution levels *["higher priority", "prioritization", "important for reasons of safety and system performance requirements", "optimal control system", "provides this protection by acting on the system's actual state, not just its operator's", col. 14, lines 24-38, "multi-channel aircraft control system", col. 2, lines 6-12, "aircraft control system", col. 6, lines 1-7, "invention relates to control systems, and more particularly to real-time control systems for which an optimized output is desired", col. 1, lines 1-6, "primary controls", "secondary controls", "priorities", "allows the plant's full range of achievable control power to be exploited by a controller", col. 18, lines 22-42].* From the reference of Dailey, it is obvious to one of ordinary skill in the art that the foreground controls of Dailey, executes at a higher execution level than the background control program because it is common knowledge that the fast, low-latency time signal path would be desired to be at a higher priority and that is why it is executed on the foreground. And vice versa, the "slower sample period" would be desired to be at a lower priority and "executed in the background" [col. 37, lines 20-27].

In addition, Daggett teaches this limitation of foreground controls with respects to high priority *["cyclically operated foreground interrupt routine 452 called SERVO", "process unscheduled or unexpected interrupts", "highest priority routine 457 called the watch dog timer interrupt functions in response to operation of the external watch dog hardware", col. 11, lines 40-53].* It would have been obvious to one of ordinary skill in the art at the time the invention

was made to include this feature of high level execution to the foreground control program for the reason of showcasing the more important aspects of the system.

Claims 3-4 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dailey (US 6,330,483 B1) as applied to claims 9 and 10 above, in view of Daggett et al. (hereinafter Daggett) (US 4,786,847), and further in view of Morshedi et al. (hereinafter Morshedi) (US 5,481,716).

10. Referring to claims 3 and 15, Dailey teaches the control processor of claims 2 and 14, respectively, wherein the supervisory control blocks include a multivariable control block including computer instructions facilitating communication or downloading of data between the control processor and a device. Dailey in view of Daggett fails to explicitly teach the device as being a workstation. However, Morshedi teaches a control system that uses a workstation *["access", "workstation 300","database", "data access", col. 4, lines 34-67, see Figure 3].* It would have been obvious to one of ordinary skill in the art at the time the invention was made to include workstations to the existing system for the reason of improving the convenience of the user. With a workstation, a user is able to access to the controls of the process control program *[col. 4, lines 34-47].*

11. Referring to claims 4 and 16, Dailey teaches the control processor of claims 3 and 15, respectively, wherein the multivariable control block includes computer instructions for

receiving and storing a process control model to be implemented by the embedded control task *["task in the embedded control software", col. 37, lines 20-28, , see examples of linear algebraic multi-variable matrices with various setpoints in col. 15, lines 50-65, "linear control system", col. 11, lines 40-44, "linear gain matrices", col. 2, lines 46-57].*

Claims 6, 8-12, 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dailey (US 6,330,483 B1) as applied to claims 9 and 10 above, in view of Daggett et al. (hereinafter Daggett) (US 4,786,847), and further in view of McManus et al. (hereinafter McManus) (US 4,788,647).

12. Referring to claims 6 and 18, Dailey in view of Draggett fails to explicitly teach the control processor of claims 5 and 17, respectively, wherein the regulatory control block is a Proportional-Integral-Derivative (PID) block. However, McManus teaches the regulatory block being a PID controller *[col. 4, lines 3-11, see Fig 2, item 120].* It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a PID control block to the existing system for the reason of increasing the control of the system by having a feedback controller such as the PID. It is well known in the art that a PID controller is generally based on the error between some user defined set point and some measured process variable.

13. Referring to claim 8, Dailey in view of Daggett fails to explicitly teach the control processor of claim 1 further comprising a repetition cycle parameter specifying a period for

re-commencing a cycle of the embedded task. However, McManus teaches having a "SUPERVISOR" that coordinates and controls, such as re-commencing, the execution of other tasks *["recommence execution until a particular message is received or flag is set", "priority scheduling", "SUPERVISOR", coordinating and controlling the execution of other tasks", col. 7, lines 7-56, "configuration parameters for specifying the repetition rate of the task", "number of a seconds before the first correction, the number of seconds between corrections", col. 16, lines 8-29].* It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of supervising the tasks for such controls as re-commencing for the reason of improving the functionality of the system. As shown in McManus, a supervisor would have certain controls such as re-commencing for the tasks and is also used to coordinate tasks with various levels of priority.

14. Referring to claim 9, McManus teaches the control processor of claim 8 wherein the set of control blocks includes a supervisory control block including a sequence of instructions to determine when to re-commence a cycle of the embedded task in accordance with a value specified by the repetition cycle parameter *["recommence execution until a particular message is received or flag is set", "priority scheduling", "SUPERVISOR", coordinating and controlling the execution of other tasks", col. 7, lines 7-56, "configuration parameters for specifying the repetition rate of the task", "number of a seconds before the first correction, the number of seconds between corrections", col. 16, lines 8-29].*

15. Referring to claim 10, Dailey in view of Daggett fails to explicitly teach the control processor of claim 1 further comprising a block processing cycle parameter specifying a repetition period for re-commencing a cycle of executing the set of control blocks. However, McManus teaches having a "SUPERVISOR" that coordinates and controls, such as re-commencing, the execution of other tasks ["recommence execution until a particular message is received or flag is set", "priority scheduling", "SUPERVISOR", coordinating and controlling the execution of other tasks", col. 7, lines 7-56, *"configuration parameters for specifying the repetition rate of the task", "number of a seconds before the first correction, the number of seconds between corrections", col. 16, lines 8-29*]. It is well known that a control system has control blocks. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of a block processing cycle parameter specifying a repetition period for re-commencing an execution cycle for the reason of improving the functionality and control of the system. As shown in McManus, a supervisor with these parameter controls would have certain controls such as re-commencing for the tasks and is also used to coordinate tasks with various levels of priority.

16. Referring to claim 11, McManus teaches the control processor of claim 10 further comprising a repetition cycle parameter specifying a period for re-commencing a cycle of executing the embedded control task tasks *["recommence execution until a particular message is received or flag is set", "priority scheduling", "SUPERVISOR", coordinating and controlling the execution of other tasks", col. 7, lines 7-56, "configuration parameters for specifying the*

repetition rate of the task", "number of a seconds before the first correction, the number of seconds between corrections", col. 16, lines 8-29].

17. Referring to claims 12 and 24, McManus teaches the control processor of claims 11 and 23, respectively, wherein a period specified by the repetition cycle parameter exceeds a period specified by the block processing cycle parameter *["sends a new message to the SUPERVISOR task whenever a full second has expired", col. 11, lines 65-68 through col. 12, lines 1-33].*

18. Referring to claim 20, Dailey in view of Daggett fails to explicitly teach the method of claim 13 further comprising the step maintaining a repetition cycle parameter specifying a period for re-commencing a cycle of the embedded task. However, McManus teaches having a "SUPERVISOR" that coordinates and controls, such as re-commencing, the execution of other tasks, which include varying the parameters for maintenance *["SUPERVISOR TASK", "configuration parameters, "this step permits these parameters to be temporarily varied during plant operation", col. 8, lines 28-50, "recommence execution until a particular message is received or flag is set", "priority scheduling", "SUPERVISOR", coordinating and controlling the execution of other tasks", col. 7, lines 7-56, "configuration parameters for specifying the repetition rate of the task", "number of a seconds before the first correction, the number of seconds between corrections", col. 16, lines 8-29].* It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of maintaining a block processing cycle parameter for re-commencing an execution cycle for the reason of improving the functionality, control and accuracy of the system. As shown in McManus, a

supervisor with these parameter controls would have certain controls such as re-commencing for the tasks and is also used to coordinate tasks with various levels of priority. It is well know that varying the parameters will allow for maintenance.

19. Referring to claim 21, McManus teaches the method of claim 20 wherein the set of control blocks includes a supervisory control block, and further comprising the step of determining, by the supervisory control block, when to re-commence a cycle of the embedded multivariable control application in accordance with a value specified by the repetition cycle parameter *["recommence execution until a particular message is received or flag is set", "priority scheduling", "SUPERVISOR", coordinating and controlling the execution of other tasks", col. 7, lines 7-56, "configuration parameters for specifying the repetition rate of the task", "number of a seconds before the first correction, the number of seconds between corrections", col. 16, lines 8-29].*

20. Referring to claim 22, Dailey in view of Daggett fails to explicitly teach the method of claim 13 further comprising the step of maintaining a block processing cycle parameter specifying a repetition period for re-commencing a cycle of executing the set of control blocks. However, McManus teaches having a "SUPERVISOR" that coordinates and controls, such as re-commencing, the execution of other tasks ["recommence execution until a particular message is received or flag is set", "priority scheduling", "SUPERVISOR", coordinating and controlling the execution of other tasks", col. 7, lines 7-56, *"configuration parameters for specifying the repetition rate of the task", "number of a seconds before the first correction, the number of*

seconds between corrections", col. 16, lines 8-29]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of a block processing cycle parameter specifying a repetition period for re-commencing an execution cycle for the reason of improving the functionality and control of the system. As shown in McManus, a supervisor with these parameter controls would have certain controls such as re-commencing for the tasks and is also used to coordinate tasks with various levels of priority.

21. Referring to claim 23, it is rejected for the same reasons as stated in the rejection of claim 20.

Claims 7 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dailey (US 6,330,483 B1) as applied to claims 9 and 10 above, in view of Daggett et al. (hereinafter Daggett) (US 4,786,847), and further in view of Westergren et al. (hereinafter Westergren) (US 5,423,076).

22. Referring to claims 7 and 19, Dailey and Draggot fails to explicitly teach the control processor of claims 5 and 17, respectively, wherein the regulatory control block is a ratio block. Fails to explicitly teach the use of ratio blocks. However, Westergren teaches using ratio blocks ["ratio blocks 146 and 147", col. 9, lines 35-68]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of ratio blocks for the reason of improving computer capabilities and calculations.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth Tang whose telephone number is (703) 305-5334. The examiner can normally be reached on 9:00am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (703) 305-8498. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is none.

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March 9, 2003

MAJID BANANKHAH
PRIMARY EXAMINER